



STP7NC80Z - STP7NC80ZFP STB7NC80Z - STB7NC80Z-1

N-CHANNEL 800V - 1.3Ω - 6.5A TO-220/FP/D²PAK/I²PAK
Zener-Protected PowerMESH™III MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP7NC80Z	800 V	< 1.5 Ω	6.5 A
STP7NC80ZFP	800 V	< 1.5 Ω	6.5 A
STB7NC80Z	800 V	< 1.5 Ω	6.5 A
STB7NC80Z-1	800 V	< 1.5 Ω	6.5 A

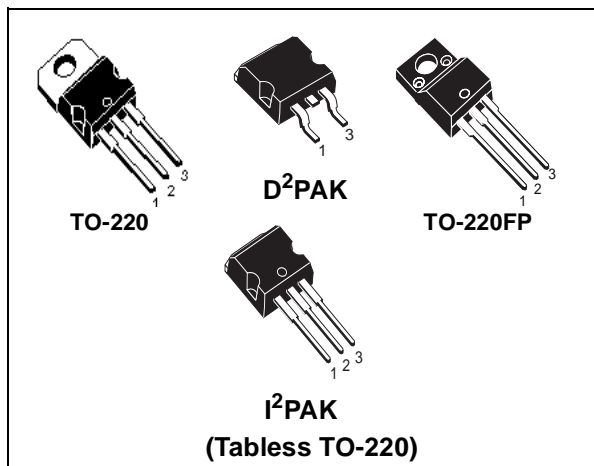
- TYPICAL R_{DS(on)} = 1.3Ω
- EXTREMELY HIGH dv/dt AND CAPABILITY
- GATE TO - SOURCE ZENER DIODES
- 100% AVALANCHE TESTED
- VERY LOW GATE INPUT RESISTANCE
- GATE CHARGE MINIMIZED

DESCRIPTION

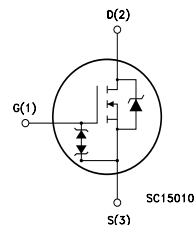
The third generation of MESH OVERLAY™ Power MOSFETs for very high voltage exhibits unsurpassed on-resistance per unit area while integrating back-to-back Zener diodes between gate and source. Such arrangement gives extra ESD capability with higher ruggedness performance as requested by a large variety of single-switch applications.

APPLICATIONS

- SINGLE-ENDED SMPS IN MONITORS, COMPUTER AND INDUSTRIAL APPLICATION
- WELDING EQUIPMENT



INTERNAL SCHEMATIC DIAGRAM



ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP7NC80Z	P7NC80Z	TO-220	TUBE
STP7NC80ZFP	P7NC80ZFP	TO-220FP	TUBE
STB7NC80ZT4	B7NC80Z	D ² PAK	TAPE & REEL
STB7NC80Z-1	B7NC80Z	I ² PAK	TUBE

STP7NC80Z - STP7NC80ZFP - STB7NC80Z - STB7NC80Z-1

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP7NC80Z STB7NC80Z STB7NC80Z-1	STP7NC80ZFP	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	800		V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	800		V
V _{GS}	Gate- source Voltage	±25		V
I _D	Drain Current (continuous) at T _C = 25°C	6.5	6.5 (*)	A
I _D	Drain Current (continuous) at T _C = 100°C	4	4(*)	A
I _{DM} (•)	Drain Current (pulsed)	26	26 (*)	A
P _{TOT}	Total Dissipation at T _C = 25°C	135	40	W
	Derating Factor	1.08	0.32	W/°C
I _{GS}	Gate-source Current	±50		mA
V _{ESD(G-S)}	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	3		KV
dv/dt	Peak Diode Recovery voltage slope	3		V/ns
V _{ISO}	Insulation Withstand Voltage (DC)	--	2000	V
T _{stg}	Storage Temperature	-65 to 150		°C
T _j	Max.Operating Junction Temperature	150		°C

(•) Pulse width limited by safe operating area

(*) Limited only by maximum temperature allowed

THERMAL DATA

		TO-220 / D ² PAK / I ² PAK	TO-220FP	
R _{thj-case}	Thermal Resistance Junction-case Max	0.93	3.13	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient Max	30		°C/W
T _I	Maximum Lead Temperature For Soldering Purpose	300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	6.5	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	290	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV _{GSO}	Gate-Source Breakdown Voltage	I _{gs} =± 1mA (Open Drain)	25			V
αT	Voltage Thermal Coefficient	T=25°C Note(3)		1.3		10 ⁻⁴ /°C
R _z	Dynamic Resistance	I _D = 20 mA,		90		Ω

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

STP7NC80Z - STP7NC80ZFP - STB7NC80Z - STB7NC80Z-1

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25°C UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	800			V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	I _D = 1 mA, V _{GS} = 0		0.9		V/°C
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 50	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±10	µA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250µA	3	4	5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 3.3 A		1.3	1.5	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} , I _D = 3.3 A		6		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		2350 164 17		pF pF pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t _{d(on)} t _r	Turn-on Delay Time Rise Time	V _{DD} = 400 V, I _D = 3 A R _G = 4.7Ω, V _{GS} = 10 V (see test circuit, Figure 3)		33 12		ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 640 V, I _D = 6 A, V _{GS} = 10V		43 12 15	58	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t _{r(Voff)} t _f t _c	Off-voltage Rise Time Fall Time Cross-over Time	V _{DD} = 640 V, I _D = 6 A, R _G = 4.7Ω, V _{GS} = 10V (see test circuit, Figure 5)		13 13 20		ns ns ns

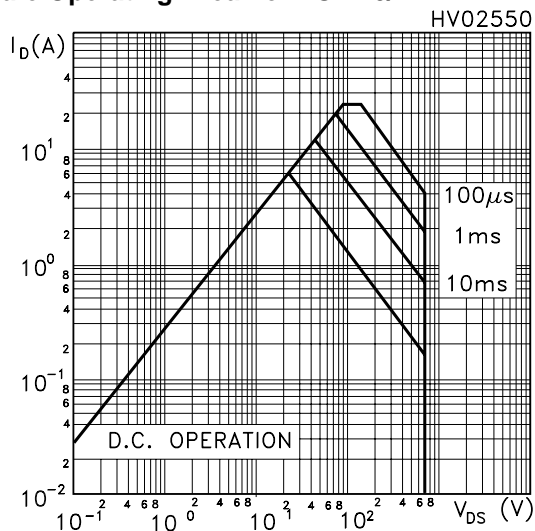
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I _{SD} I _{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				6.5 26	A A
V _{SD} (1)	Forward On Voltage	I _{SD} = 6.1 A, V _{GS} = 0			1.6	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I _{SD} = 6 A, di/dt = 100A/µs V _{DD} = 40V, T _J = 150°C (see test circuit, Figure 5)		680 6 18		ns µC A

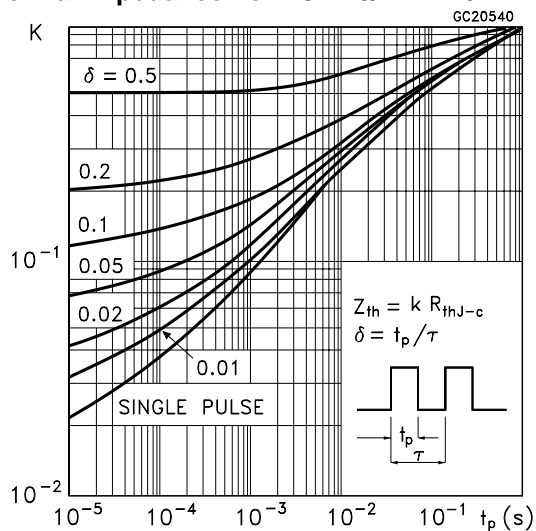
Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.
3. ΔV_{BV} = αT(25°-T) BV_{GSO}(25°)

STP7NC80Z - STP7NC80ZFP - STB7NC80Z - STB7NC80Z-1

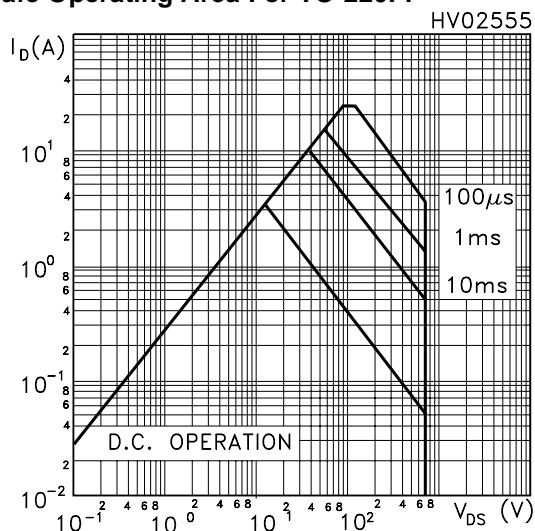
Safe Operating Area For TO-220/I2PAK



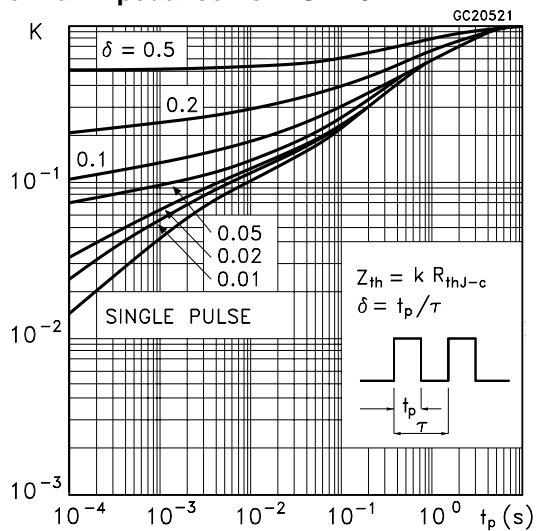
Thermal Impedance For TO-220/D2PAK/I2PAK



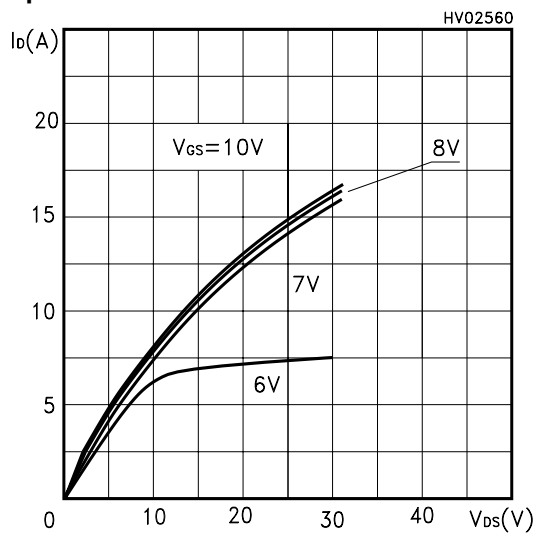
Safe Operating Area For TO-220FP



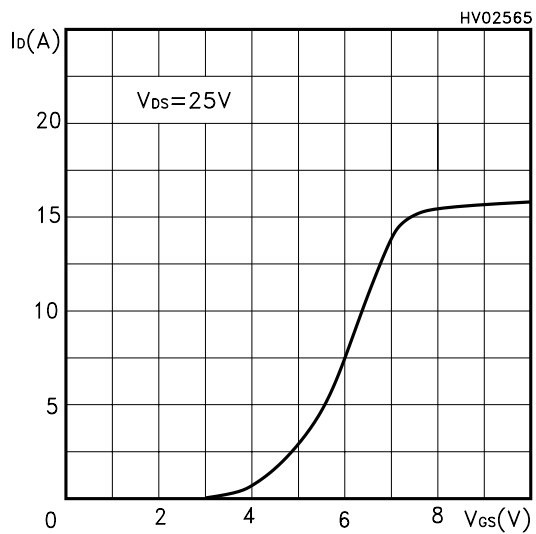
Thermal Impedance For TO-220FP



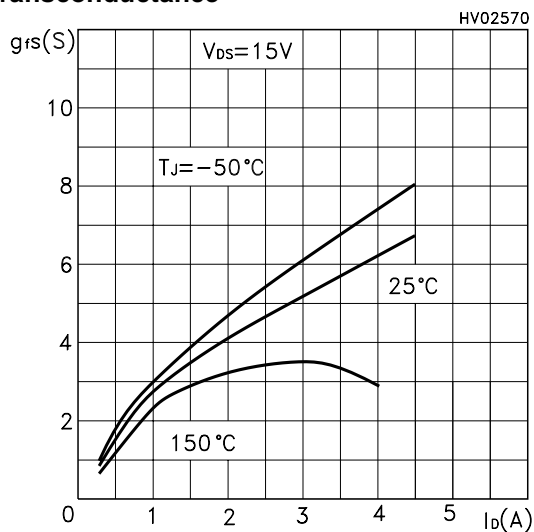
Output Characteristics



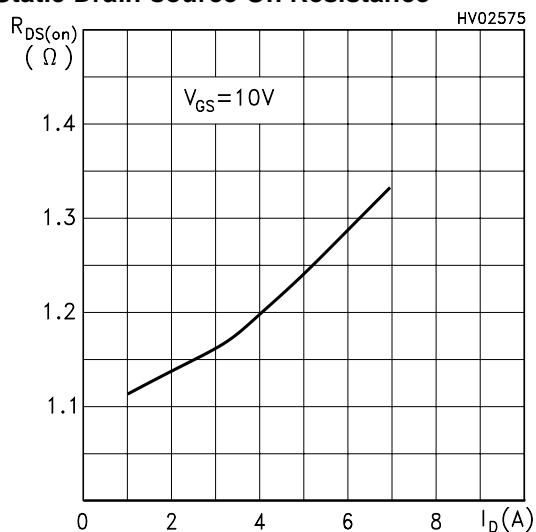
Transfer Characteristics



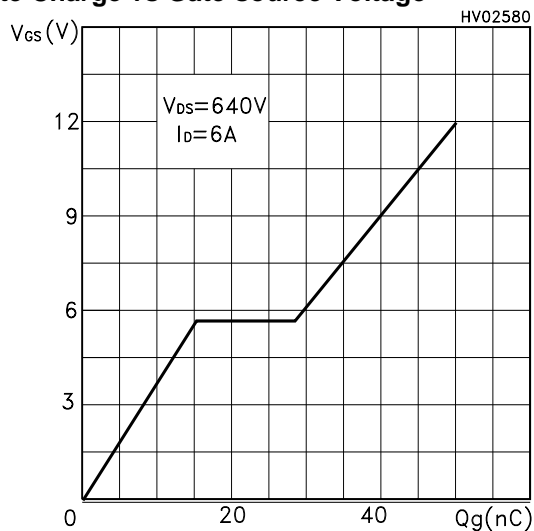
Transconductance



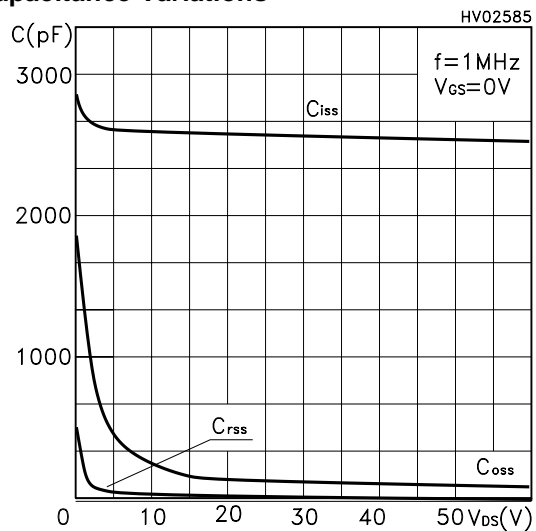
Static Drain-source On Resistance



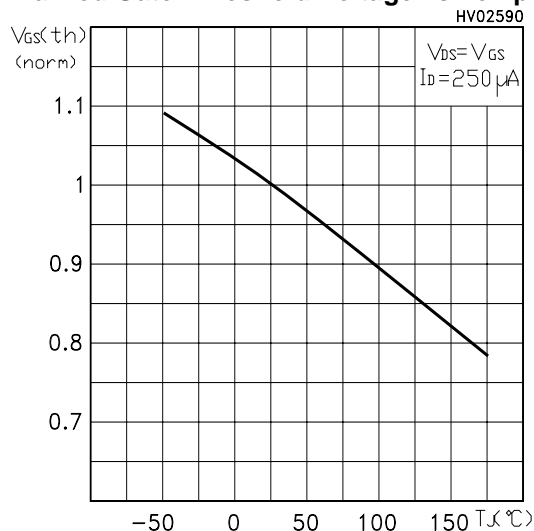
Gate Charge vs Gate-source Voltage



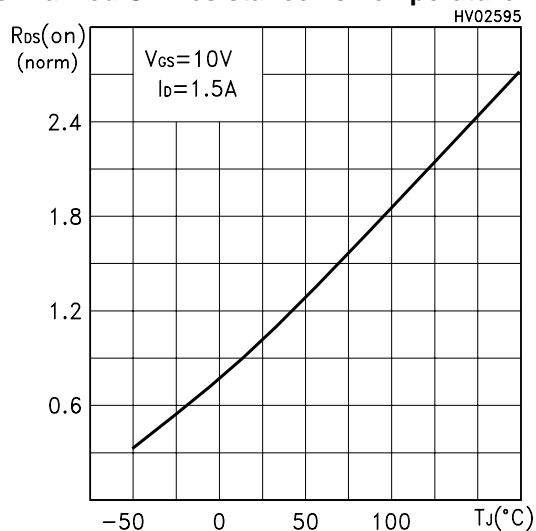
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

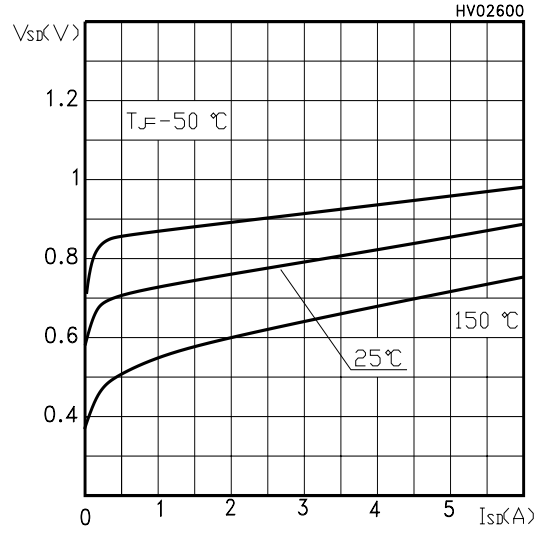


Fig. 1: Unclamped Inductive Load Test Circuit

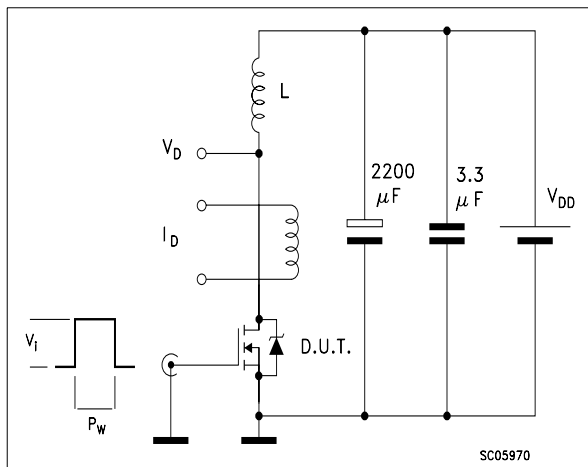


Fig. 2: Unclamped Inductive Waveform

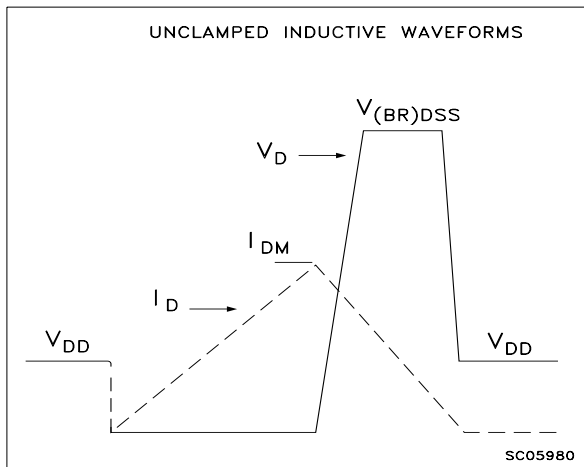


Fig. 3: Switching Times Test Circuit For Resistive Load

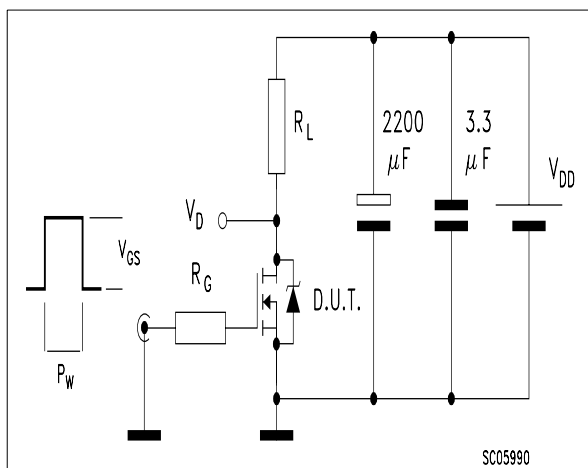


Fig. 4: Gate Charge test Circuit

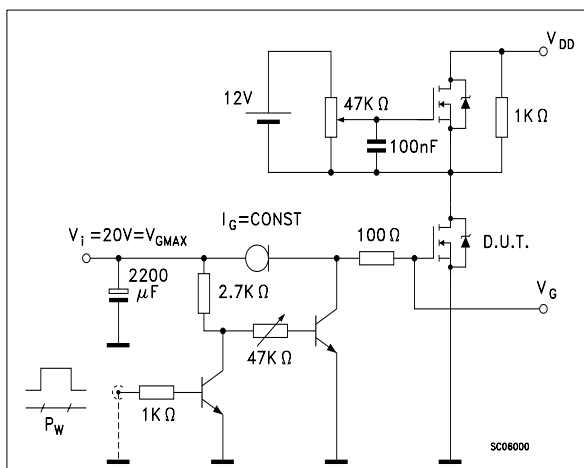
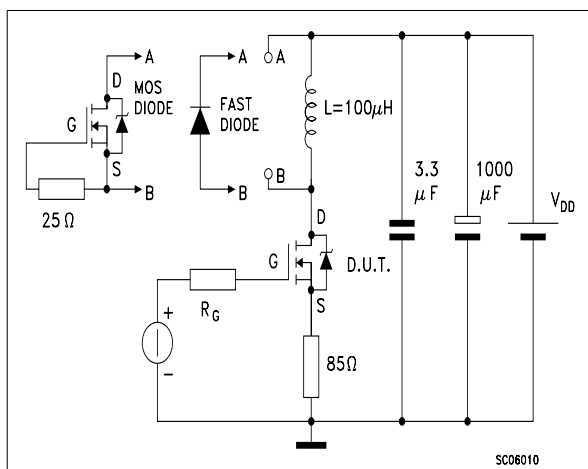
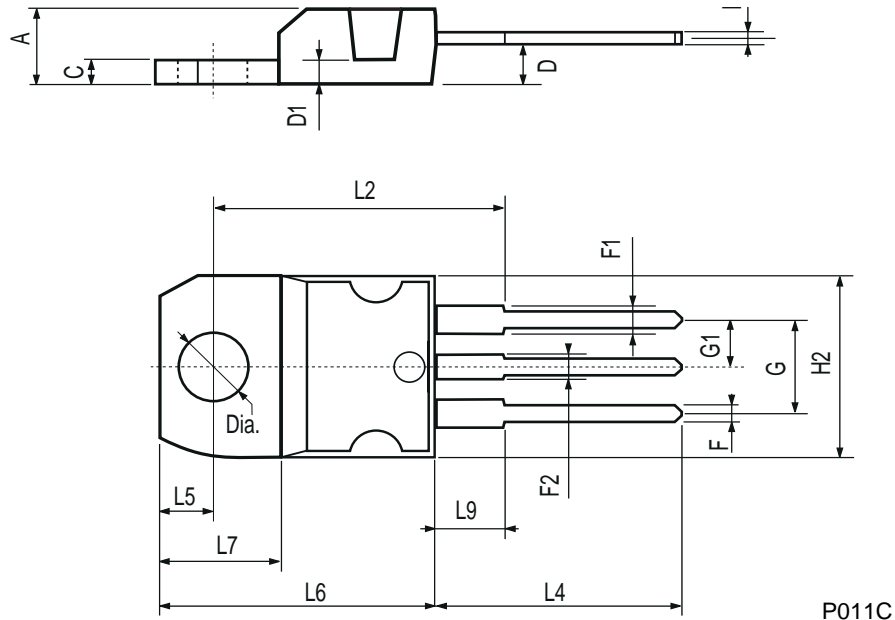


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



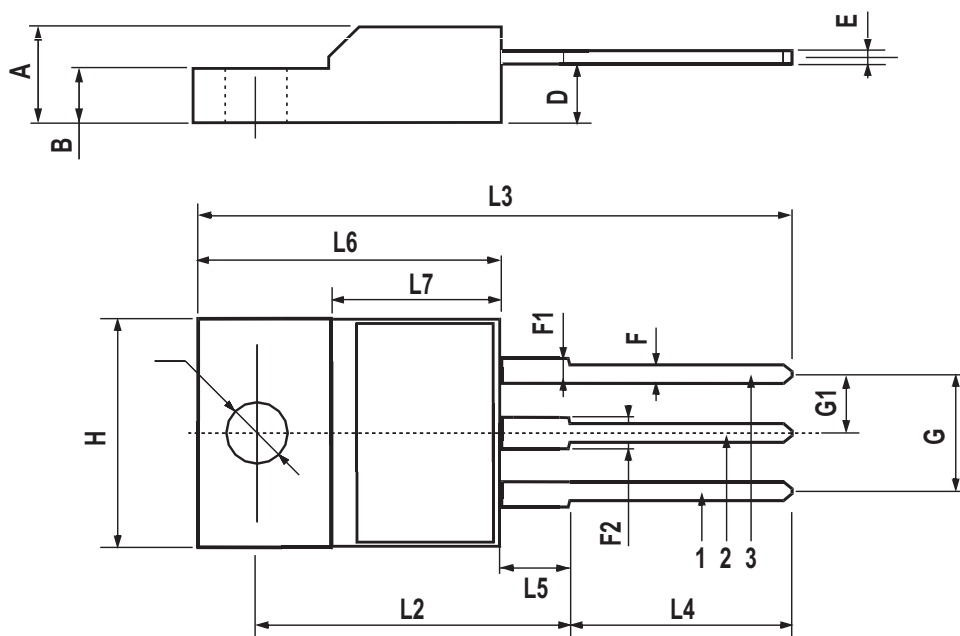
TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



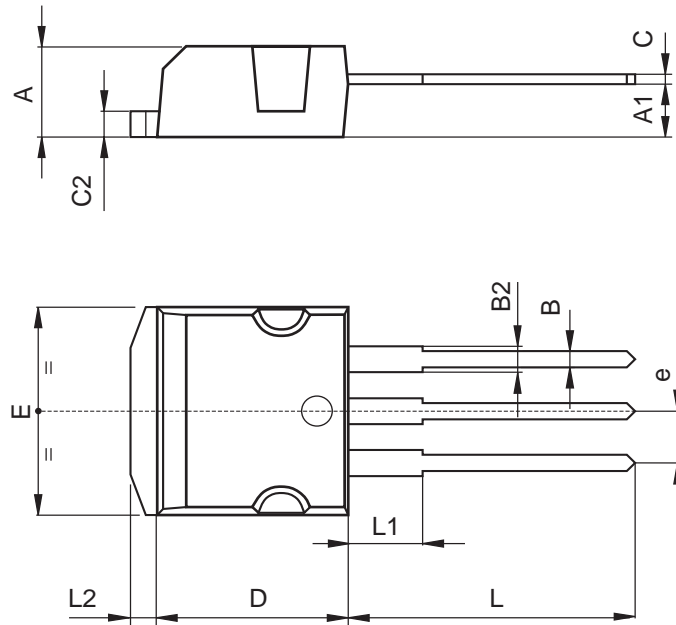
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.5	0.045		0.067
F2	1.15		1.5	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-262 (I²PAK) MECHANICAL DATA

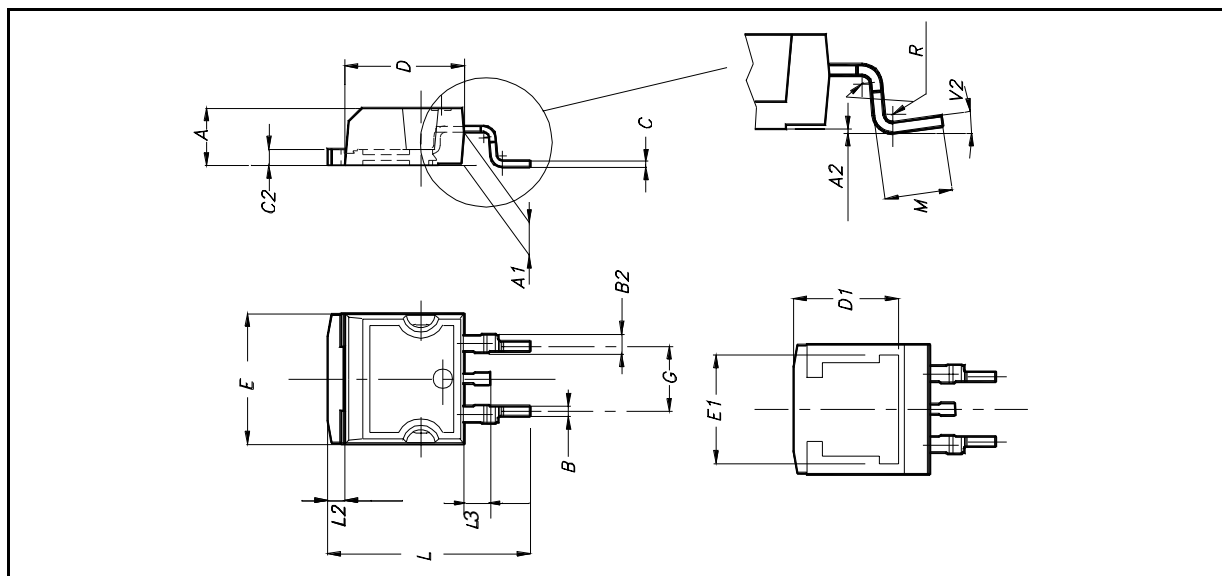
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
e	2.4		2.7	0.094		0.106
E	10		10.4	0.393		0.409
L	13.1		13.6	0.515		0.531
L1	3.48		3.78	0.137		0.149
L2	1.27		1.4	0.050		0.055

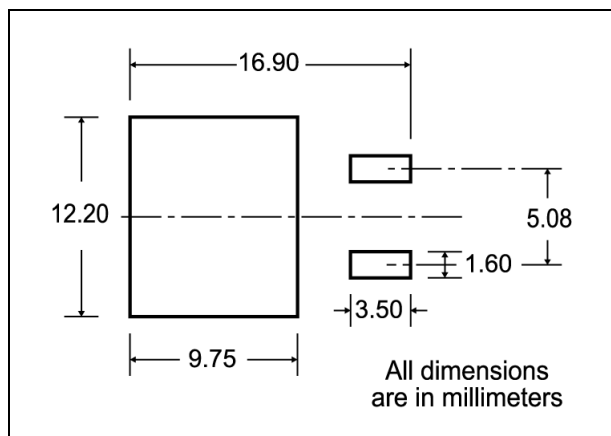
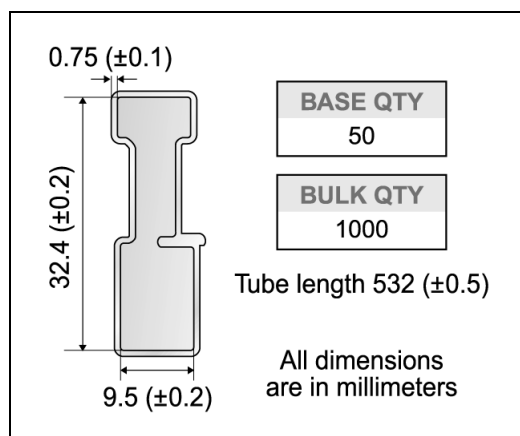
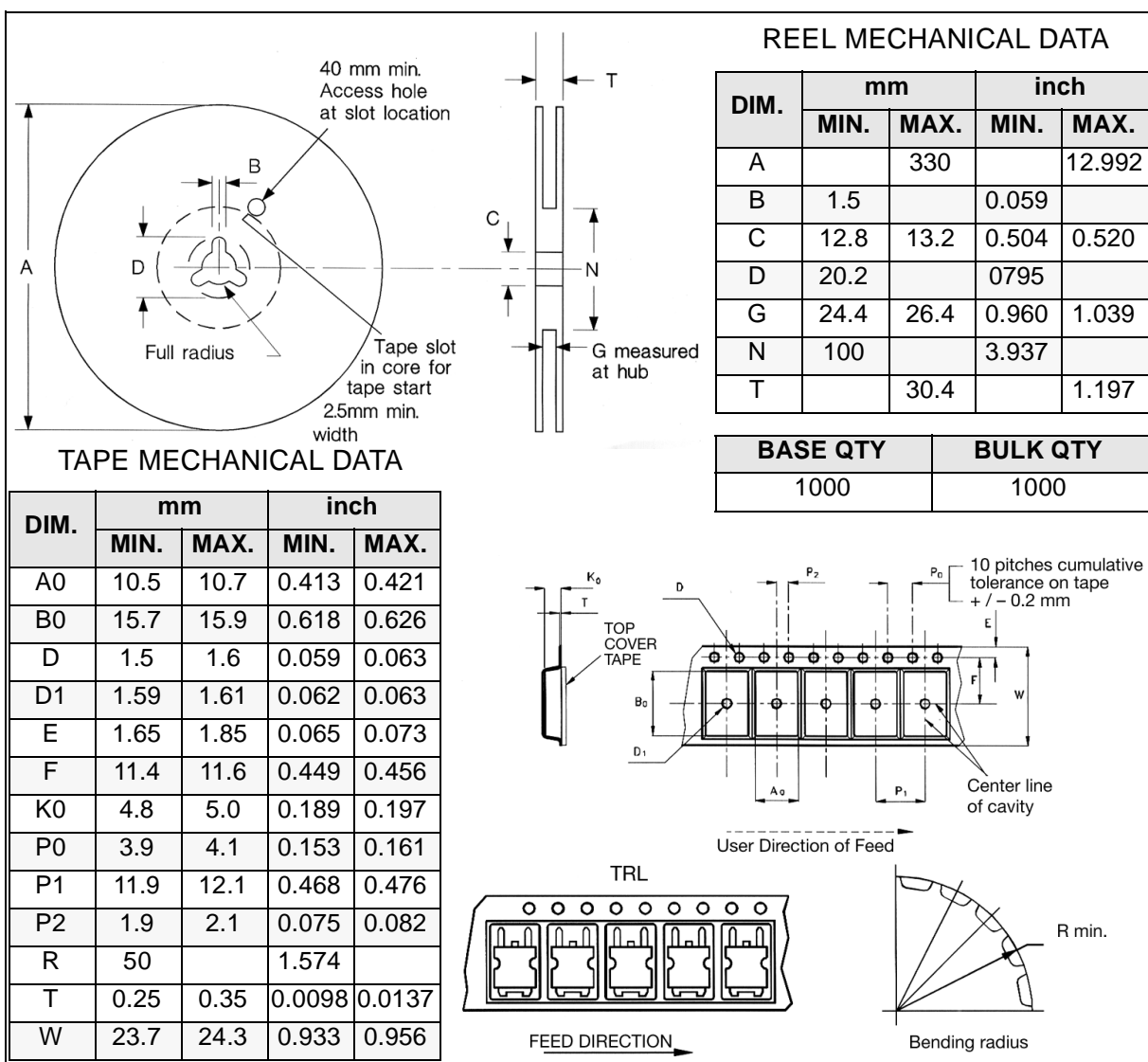


P011P5/E

D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



D²PAK FOOTPRINT**TUBE SHIPMENT (no suffix)*****TAPE AND REEL SHIPMENT (suffix "T4")***

* on sales type

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2003 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>